

IO-Link Safety Device Stack

With the TEConcept IO-Link Safety Device Stack, manufacturers of safety sensors and actuators integrate IO-Link Safety communication (IEC 61139-2, up to SIL3 / PL_e) directly into their devices. The Safety Communication Layer operates as a black channel on standard IO-Link and is fieldbus-independent: one FS device for all FSCPs such as PROFIsafe, CIP Safety or FSoE. The stack comprises [SCL, device state machines, OSSDe start-up behaviour, ...], supports [MCU platforms] and is delivered with [safety manual, IODD example, integration support]. Developed to [IEC 61508-3 / certification status]. Test equipment and assessment support from a single source.

Implementation

Here is what the technical implementation looks like: the TEConcept IO-Link Safety Device Stack is delivered embedded in a demo application – a fully functional IO-Link Safety device. The core safety components are developed and assessed to IEC 61508-3 (SIL3) and enter your assessment unchanged. The demo application shows one example of how a future safety device can be structured.

Hardware

The system can be implemented as a single-channel 1oo1 or a dual-channel redundant 1oo2 architecture. The 1oo2 variant with a second safety CPU (S-Guest) increases diagnostic coverage and supports higher safety requirements.

Architecture

The actual safety function is performed by the Safety Communication Layer (SCL); the Safety Layer Manager (SLM) handles configuration. Both components are developed to IEC 61508-3 and are adopted unchanged. Ready-made modules for cyclic and acyclic data transfer are available for communication between the processors. They form the transmission path (black channel) and can either be adopted as they are or replaced with your own components.

The underlying physical layer is exchangeable and is adapted to the respective hardware.

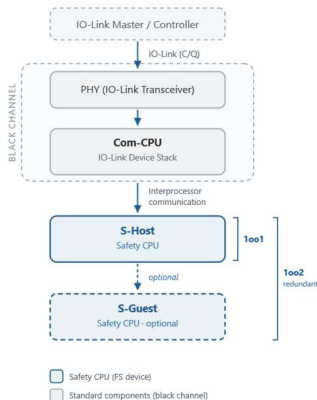
The safety application demonstrates how a safety sensor or actuator can be built on this foundation. This part is intended as a template and is modified as required.

Footprint

The size of the compiled code depends heavily on the configuration used and on compiler optimisation. The following figures serve as a guide.

S-Host/S-Guest: 38k Flash, 6k RAM Com-CPU: 23k Flash, 4k RAM

Example hardware setup



Software architecture, safety CPU

